150

AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No. 13434US01

In the Application of:

Oscar E. Agazzi

U.S. Serial No.: 09/557,274

Filed: April 24, 2000

For: PHY CONTROL MODULE FOR A MULTI-PAIR GIGABIT TRANSCEIVER

Examiner: Liu Shuwang

Group Art Unit: 2634

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail, postage prepaid, in an envelope addressed to: MS: APPEAL BRIEF-PATENTS, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on October 19, 2004.

John A. Wiberg
Reg. No. 44,401

BRIEF ON APPEAL

MAIL STOP: APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from an Office Action dated May 19, 2004, in which claims 1-8 and 15-22 were finally rejected.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 010763, frame 0692.

RELATED APPEALS AND INTERFERENCES

There currently are no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-8 and 15-22 are pending in the present application. Claims 9-14 are cancelled. Pending claims 1-8 and 15-22 have been rejected under 35 U.S.C. § 102(e) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

The present invention relates to a PHY control module for controlling operation in a gigabit Ethernet transceiver that includes more than one constituent transceiver. The IEEE 802.3ab standard (also called 1000BASE-T) for 1 gigabit per second (Gb/s) Ethernet full-duplex communication system specifies that there are four constituent transceivers in a gigabit transceiver and that the full-duplex communication is over four twisted pairs of Category-5 copper cables. Since a Gigabit Ethernet transceiver has four constituent transmitters and four constituent receivers, its operation is much more complex than the operation of a traditional full-duplex transceiver. Power consumption is an important problem that must be addressed. The four twisted pairs of cable may introduce different delays on the signals, causing the signals to have different phases. This, in turn, requires the gigabit Ethernet transceiver to have four A/D converters operating in accordance with four respective sampling clock signals. In addition, the problem of switching noise coupled from the digital signal processing blocks of the gigabit Ethernet transceiver to the four A/D converters must also be addressed. Therefore, there is a need to have an efficient Physical (PHY) Control module for controlling the complex operation of a gigabit Ethernet transceiver.

According to the present invention, a Physical Layer control module (PHY control module) controls operation of a multi-pair gigabit transceiver that further comprises a Physical Coding Sublayer module (PCS module) and a digital signal processing module (DSP). The PHY control module receives user-defined inputs from a serial management module and status signals from the DSP and the PCS module. The PHY control module generates control signals responsive to the user-defined inputs and the status signals. The control signals are provided to the DSP and the PCS module.

Claim 1 is directed to a method for controlling operation of a multi-pair gigabit transceiver, the multi-pair gigabit transceiver comprising a Physical Layer control module (PHY control module), a Physical Coding Sublayer module (PCS module) and a digital signal processing module (DSP). According to the method, the PHY control module receives user-defined inputs from a serial management module and status signals from the DSP and the PCS module. The PHY control module generates control signals responsive to the user-defined inputs and the status signals. The control signals are provided to the DSP and the PCS module.

The invention of claim 1 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. Referring to FIG. 13, the PHY control module 1302 receives user-defined inputs 1304 from a serial management module 1306 and status signals 1318 from the DSP and the PCS module 1320. The PHY control module 1302 generates control signals 1322 responsive to the user-defined inputs 1304 and the status signals 1318. The control signals 1322 are provided to the DSP and the PCS module 1320.

Claim 2 is directed to the method of claim 1, wherein the multi-pair gigabit transceiver further comprises an auto-negotiation module. The method further comprises receiving at the PHY control module a link control signal from the auto-negotiation module to start operation of the PCS module and the DSP.

The invention of claim 2 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. FIG. 13 shows an auto-negotiation module 1310 that provides a link control signal 1308 to the PHY control module 1302 to start operation of the PCS module and the DSP 1320. See, e.g., p. 38, lines 27–28.

Claim 3 is directed to the method of claim 1, wherein the multi-pair gigabit transceiver further comprises a Gigabit Medium Independent Interface (GMII) module. The method further comprises receiving at the PHY control module a transmit enable signal from the GMII module to start transmission of data packets.

The invention of claim 3 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. FIG. 13 shows a Gigabit Medium Independent Interface (GMII) module 1314 that provides a transmit enable signal 1312 to the PHY control module 1302 to start transmission of data packets. See, e.g., p. 39, lines 1-2.

Claim 4 is directed to the method of claim 1 and further comprises receiving a user-defined reset signal at the PHY control module, and generating a control signal to reset the DSP and the PCS module.

The invention of claim 4 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. Page 38, lines 13-15 states that the PHY control module 1302 can receive a user-defined reset signal 1316 to reset the DSP and PCS modules 1320.

Claim 5 is directed to the method of Claim 1 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS module.

The invention of claim 5 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. See, e.g., page 39, lines 3-4.

Claim 6 is directed to the method of Claim 1 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

The invention of claim 6 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. See, e.g., page 39, lines 5-7.

Claim 7 is directed to the method of Claim 1 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

The invention of claim 7 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. See, e.g., page 39, lines 5-7.

Claim 8 is directed to the method of Claim 1 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.

The invention of claim 8 is described in the Specification of the present application at, for example, page 38, line 7 – page 40, line 13. See, e.g., page 39, lines 5-7.

Claim 15 is directed to a PHY control module for controlling operation of a multi-pair Ethernet transceiver, the multi-pair Ethernet transceiver comprising a Physical Coding Sublayer module (PCS module) and a Digital Signal Processing module (DSP). The PHY control module comprises a main state machine configured to receive user-defined inputs from a serial management module and status signals from the DSP and the PCS module, to generate control signals responsive to the user-defined inputs and the status signals, and to provide the control signals to the DSP and the PCS module.

The invention of claim 15 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. Referring to FIG. 13, the PHY control module 1302 receives user-defined inputs 1304 from a serial management module 1306 and status signals 1318 from the DSP and the PCS module 1320. The PHY control module 1302 generates control signals 1322 responsive to the user-defined inputs 1304 and the status signals 1318. The control signals 1322 are provided to the DSP and the PCS module 1320. Referring to FIG. 14, the PHY control module 1302 includes a main state machine 1402 which controls operations of a set of substate machines.

Claim 16 is directed to the PHY control module of claim 15, wherein the multi-pair gigabit transceiver further comprises an auto-negotiation module. The main state machine further receives a link control signal from the auto-negotiation module to start operation of the PCS module and the DSP.

The invention of claim 16 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. FIG. 13 shows an auto-negotiation module 1310 that provides a link control signal 1308 to the PHY control

module 1302 to start operation of the PCS module and the DSP 1320. See, e.g., p. 38, lines 27–28.

Claim 17 is directed to the PHY control module of claim 15, wherein the multi-pair gigabit transceiver further comprises a Gigabit Medium Independent Interface (GMII) module. The PHY control module receives a transmit enable signal from the GMII module to start transmission of data packets.

The invention of claim 17 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. FIG. 13 shows a Gigabit Medium Independent Interface (GMII) module 1314 that provides a transmit enable signal 1312 to the PHY control module 1302 to start transmission of data packets. See, e.g., p. 39, lines 1-2.

Claim 18 is directed to the PHY control module of claim 15 wherein the main state machine receives a user-defined reset signal and generates a control signal to reset the DSP and the PCS module.

The invention of claim 18 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. Page 38, lines 13-15 states that the PHY control module 1302 can receive a user-defined reset signal 1316 to reset the DSP and PCS modules 1320.

Claim 19 is directed to the PHY control module of claim 15 wherein the control signals include a DSP/PCS reset signal to reset the DSP and the PCS module.

The invention of claim 19 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. See, e.g., page 39, lines 3-4.

Claim 20 is directed to the PHY control module of claim 15 wherein the DSP comprises a set of echo cancellers and a set of near-end cross-talk (NEXT) cancellers, and wherein the control signals include echo and NEXT control signals to control convergence of the echo cancellers and NEXT cancellers, respectively.

The invention of claim 20 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. See, e.g., page 39, lines 5-7.

Claim 21 is directed to the PHY control module of claim 15 wherein the DSP comprises a multi-dimensional decision feedback equalizer (DFE) and wherein the control signals include DFE control signals to control convergence of the multi-dimensional DFE.

The invention of claim 21 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. See, e.g., page 39, lines 5-7.

Claim 22 is directed to the PHY control module of claim 15 wherein the DSP comprises a timing recovery (TR) module and wherein the control signals include TR control signals to control convergence of the timing recovery module.

The invention of claim 22 is described in the Specification of the present application at, for example, page 38, line 7 – page 41, line 26. See, e.g., page 39, lines 5-7.

ISSUES FOR REVIEW

I. Are claims 1-8 and 15-22 unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,377,640 issued to Francois Trans?

GROUPING OF CLAIMS

The claims do not stand or fall together.

Claims 1-8 stand or fall together.

Claims 15-22 stand or fall together, and are believed to be separately patentable from claims 1-8, as will be explained in the following argument section.

ARGUMENT

I. Claims 1-8 and 15-22 are not anticipated under 35 U.S.C. § 102(e) by Trans (US 6,377,640).

In the Office Action of May 19, 2004, the Examiner rejected claims 1-8 and 15-22 under 35 U.S.C. § 102(e) as being anticipated by Trans (US 6,377,640). 35 U.S.C. 102(e) states:

> A person shall be entitled to a patent unless... the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[1]

A. Claims 1-8 are not anticipated under 35 U.S.C. § 102(e) by Trans (US 6,377,640) because Trans does not teach each and every element of claim 1.

Claim 1 is directed to:

> 1. A method for controlling operation of a multi-pair gigabit transceiver, the multi-pair gigabit transceiver comprising a Physical Layer control module (PHY control module), a Physical Coding Sublayer module (PCS module) and a digital signal processing module (DSP), the method comprising:
>
> receiving at the PHY control module user-defined inputs from a serial management module and status signals from the DSP and the PCS module;
>
> generating, at the PHY control module, control signals responsive to the user-defined inputs and the status signals; and
>
> providing the control signals to the DSP and the PCS module.

[1] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In the Office Action of May 19, 2004, the Examiner asserts that Trans discloses a Physical Layer control module (PHY control module), as called for in claim 1.[2] The Examiner deems the status and control registers 328 and the auto-negotiation function 329 in Figure 3, or the control register, status register and power register in Figure 1D, to constitute such a PHY control module. Applicant submits that the auto-negotiation function 329 of Trans does not constitute a PHY control module. Indeed, the present invention includes an auto-negotiation module 1310, and this module is separate from the PHY control module 1302.[3] Furthermore, a register or set of registers such as the status and control registers 328 do not, by themselves, constitute a control module.

The Examiner also asserts that Tran's 4B/5B encoder 322, serial scrambler 323, MLT3/PAM-5 encoder 324, 10B/PAM map 325, partial response modulator 327, PAM/10B map 331 and quinary encoder 333 constitute a PCS module as called for in claim 1.[4] Although Applicant does not necessarily agree with this conclusion, Applicant will show in the argument that follows that these elements in Trans do not interact with the elements that the Examiner deems to constitute a PHY control module, in the manner called for in claim 1.

The Examiner also asserts that the transmitter 342 in Figure 3 of Trans constitutes a digital signal processor as called for in claim 1.[5] Applicant submits that the transmitter 342 is not a digital signal processor, and is nowhere referred to in the specification as a digital signal processor. The transmitter 342 resides in the analog section 34 of the transceiver chip shown in Figure 3 of Trans, further supporting the conclusion that the transmitter 342 is not is digital signal processor.

The Examiner also asserts that Trans discloses a PHY control module receiving user-defined input signals from a serial management module, as called for in claim 1.[6] The Examiner deems the serial scrambler 323 and MLT3/PAM-5 encoder 324 of Figure 3 of Trans to constitute a serial management module. Applicant submits that neither serial scrambler 323 nor MLT3/PAM-5 encoder 324 provide any communication to the control registers 328 or the auto-negotiation function 329, which are the elements that the

[2] 5/19/04 Office Action, p. 4, referring to Figure 3 and col. 58, lines 16-65 of Trans.
[3] Present application, p. 38, lines 7-28, referring to Figure 13.
[4] 5/19/04 Office Action, p. 4.
[5] 5/19/04 Office Action, p. 4.

Examiner deems to constitute a PHY control module. Therefore, Trans does not disclose a PHY control module receiving user defined-inputs from a serial management module, as called for in claim 1.

The Examiner also asserts that Trans discloses a PHY control module receiving status signals from a PCS module, as called for in claim 1.[7] As mentioned previously, Examiner deems elements 322, 323, 324, 325, 327, 331 and 333 of Figure 3 of Trans to constitute a PCS module. Applicant submits that none of these elements 322, 323, 324, 325, 327, 331 and 333 provide status signals (or any other signals) to the control registers 328 or the auto-negotiation function 329, which are the elements that the Examiner deems to constitute a PHY control module. Therefore, Trans does not disclose a PHY control module receiving status signals from a PCS module, as called for in claim 1.

The Examiner also asserts that Trans discloses a PHY control module receiving status signals from a DSP, as called for in claim 1.[8] As mentioned previously, Examiner deems the transmitter 342 of Figure 3 of Trans to constitute a DSP. Applicant submits that the transmitter 342 does not provide status signals (or any other signals) to the control registers 328 or the auto-negotiation function 329, which are the elements that the Examiner deems to constitute a PHY control module. Therefore, Trans does not disclose a PHY control module receiving status signals from a DSP, as called for in claim 1.

The Examiner also asserts that Trans discloses generating, at a PHY control module, control signals responsive to the aforementioned user-defined inputs and status signals.[9] As demonstrated above, the elements of Trans that the Examiner deems to be a PHY control module, namely control registers 328 and auto-negotiation function 329, do not receive said user-defined inputs and status signals, and therefore the control registers 328 and auto-negotiation function 329 cannot generate control signals responsive to said user-defined inputs and status signals.

The Examiner also asserts that Trans discloses that the PHY control module provides generated control signals to the DSP.[10] Applicant submits that Trans' control registers 328 and auto-negotiation function 329, which are the elements deemed by the

---

[6] 5/19/04 Office Action, p. 5.
[7] 5/19/04 Office Action, p. 5.
[8] 5/19/04 Office Action, p. 5.
[9] 5/19/04 Office Action, p. 5.

Examiner to constitute a PHY control module, do not provide control signals (or any signals) to the transmitter 342, which is the element that the Examiner deems to constitute a DSP. Therefore, Trans does not disclose a PHY control module providing control signals to a DSP, as called for in claim 1.

The Examiner also asserts that Trans discloses that the PHY control module provides generated control signals to the PCS module.[11] Applicant submits that Trans' control registers 328 and auto-negotiation function 329, which are the elements deemed by the Examiner to constitute a PHY control module, do not provide control signals (or any signals) to any of elements 322, 323, 324, 325, 327, 331 and 333, which are the elements that the Examiner deems to constitute a PCS module. Therefore, Trans does not disclose a PHY control module providing control signals to a PCS module, as called for in claim 1.

Because Trans does not teach any of the limitations discussed above, let alone *every* limitation contained in claim 1, Trans does not anticipate claim 1, nor claims 2-8, which depend on claim 1.

[10] 5/19/04 Office Action, p. 5.
[11] 5/19/04 Office Action, p. 5.

B. Claims 15-22 are not anticipated under 35 U.S.C. § 102(e) by Trans (US 6,377,640) for the reasons discussed above with respect to claim 1, and further because Trans does not disclose a PHY control module including a state machine.

Claim 15 is directed to:

> 15. A PHY control module for controlling operation of a multi-pair Ethernet transceiver, the multi-pair Ethernet transceiver comprising a Physical Coding Sublayer module (PCS module) and a Digital Signal Processing module (DSP), the PHY control module comprising:
>
> a main state machine configured to receive user-defined inputs from a serial management module and status signals from the DSP and the PCS module, to generate control signals responsive to the user-defined inputs and the status signals, and to provide the control signals to the DSP and the PCS module.

Applicant submits that claim 15 distinguishes over Trans for all of the reasons discussed in Section I.A of this Appeal Brief, and further because Trans does not disclose a PHY control module that includes a state machine, as is called for in claim 15. The Examiner asserts in the Office Action that the PHY control module of claim 15 is taught by the control and status registers 328 and auto-negotiation function 329 in Figure 3 of Trans or by the control register, status register and power register in Figure 1D.[12] Applicant submits that none of these registers include a state machine and therefore cannot constitute a PHY control module as called for in claim 15. For this reason, and for the reasons set out above with respect to claim 1, Trans does not anticipate claim 15, nor claims 16-22, which depend on claim 15.

II. CONCLUSION

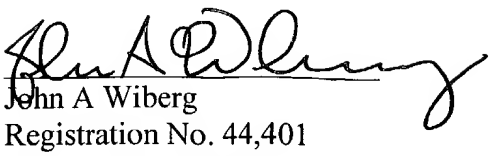
For the foregoing reasons, claims 1-8 and 15-22 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

[12] 5/19/04 Office Action, p. 4.

Dated: October 19, 2004

Respectfully submitted,



John A Wiberg
Registration No. 44,401
Attorney for appellant

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, IL 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100